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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,690	11/29/2001	James Y.C. Chang	1875.1210003/RES/JTH	9803

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EXAMINER

PHAM, TUAN

ART UNIT	PAPER NUMBER
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2643

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/995,690

Applicant(s)

CHANG, JAMES Y.C.

Examiner

TUAN A. PHAM

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 5-6, and 9-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>5/10/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Applicant's remark, filed on 04/25/2005, with respect to the rejection(s) of claim(s) 1-10 under 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made with Khoury et al. (U.S. Patent No.: 5,532,637) in view of Chadwick et al. (U.S. Patent No.: 4,628,518).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 5/10/2005 has been considered by Examiner and made of record in the application file.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury et al. (U.S. Patent No.: 5,532,637, hereinafter, "Khoury") in view of Chadwick et al. (U.S. Patent No.: 4,628,518, hereinafter, "Chadwick").**

Regarding claim 1, Khoury teaches a mixer circuit (see figure 3), comprising: a

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signal input (see figure 3, I/P2+, I/P2-); an RF transconductance circuit that is configured to convert an input differential signal received at said signal input to a differential current (see figure 3, transistor 11, transistor 12, current I1 flow from transistor 15 to transistor 11, Current I2 flow from transistor 17 to transistor 12, col.3, ln.25-67, col.4, ln.1-47), said RF transconductance circuit having a pair of field effect transistors (see figure 3, transistor 11, transistor 12, col.3, ln.25-67); a LO switching circuit configured to switch said differential current between outputs of said mixer circuit at a rate determined by a differential LO signal (see figure 3, transistors 15-18, O/P+, O/P-, col.3, ln.25-67, col.4, ln.1-47), and a variable current source that adds a DC current to said pair of field effect transistors in said RF transconductance circuit the DC current adjusted so as to reduce noise in the mixer circuit (see figure 3, current control circuit 32, VCC variable current source that add the DC current to pairs of transistor 11, 12 to reduce the noise, col.3, ln.25-67, col.4, ln.1-47).

It should be noticed that Khoury fails to teach how to reduce the flicker noise in the mixer. However, Chadwick teaches such feature (see col.4, ln.35-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chadwick into view of Khoury in order to reduce cost as suggested by Chadwick at column 2, lines 7-12.

Regarding claim 6, Khoury teaches a mixer circuit (see figure 3), comprising: a signal input (see figure 3, I/P2+, I/P2-); an RF transconductance circuit that is configured to convert an input differential signal received at said signal input to a differential current (see figure 3, transistor 11, transistor 12, current I1 flow from

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transistor 15 to transistor 11, Current I2 flow from transistor 17 to transistor 12, col.3, ln.25-67, col.4, ln.1-47) said RF transconductance circuit having a pair of field effect transistors (see figure 7, transistor 11, transistor 12, col.3, ln.25-67); a LO switching circuit configured to switch said differential current between outputs of said mixer circuit at a rate determined by a differential LO signal (see figure 3, transistors 15-18, O/P+, O/P-, col.3, ln.25-67, col.4, ln.1-47); a first variable current source configured to add a first DC current to a first FET of said pair of FETs (see figure 3, first variable current source 25, FET 11, 12); and a second variable current source configured to add a second DC current to a second FET of said pair of FETs (see figure 3, second variable current source 26, FET 11, 12, col.3, ln.25-67, col.4, ln.1-47, it is inherent that both variable current source 25 and 26 are added the DC current to a pairs of transistor 11 and 12), wherein the first DC current and the second DC current are determined so as to minimize noise of the mixer circuit (see figure 1, col.3, ln.25-67, col.4, ln.1-47).

It should be noticed that Khoury fails to teach how to reduce the flicker noise in the mixer. However, Chadwick teaches such feature (see col.4, ln.35-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chadwick into view of Khoury in order to reduce cost as suggested by Chadwick at column 2, lines 7-12.

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5. Claims 5, and 9-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury et al. (U.S. Patent No.: 5,532,637, hereinafter, "Khoury") in view of Chadwick et al. (U.S. Patent No.: 4,628,518, hereinafter, "Chadwick") as applied to claims 1 and 6 above, and further in view of Kung (U.S. Patent No.: 6,037,825).

Regarding claims 5 and 9, Khoury and Chadwick, in combination, fails to teach the mixer circuit wherein said DC current bypasses said LO switching circuit. However, Kung teaches such features (see col.4, ln.35-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kung into view of Khoury and Chadwick in order to improve the noise by reducing the DC current as suggested by Kung at column 1, lines 55-59.

Regarding claim 10, Kung further teaches the mixer circuit wherein said first DC current is added to a drain of said first FET in said pair of FETs, and said second DC current is added to a drain of said second FET in said pair of FETs (see figure 7, first current 24, second current 25, transistors 11, 12).

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Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tuan A. Pham** whose telephone number is (571) 272-8097. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Curtis Kuntz can be reached on (571) 272-7499 and

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have question on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 2643
July 2, 2005
Examiner

Tuan Pham


CURTIS KUNTZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600